WHAT IS CLAIMED IS:

1. A delay circuit comprising:

a delay section having two or more predetermined delay stages in which predetermined delay time is added to an input signal; and

selecting switch sections for combining the predetermined delay stages as appropriate and establishing a delay path for the input signal that outputs a delayed output signal having the desired delay time, wherein

the selecting switch sections comprise:

buffer sections for inputting propagated signals from the input signal; and

selecting sections for activating the buffer sections when the delay path is being established in the delay section.

2. The delay circuit according to claim 1, wherein, in the delay section, the predetermined delay stages are provided with individual delayed output terminals for outputting individual delayed output signals having the predetermined delay times, and selecting switch sections are provided for each individual delayed output terminals with input terminals of the buffer sections in the selecting switch sections being connected to the individual delayed output terminals and output terminals of the selecting switch sections being mutually joined.

3. The delay circuit according to claim 1, wherein, in the delay section, the predetermined delay stages are provided with individual delay input terminals for inputting signals to which the predetermined delay times are to be added, and the rise delay time and fall delay time for the input signals are balanced so as to be substantially uniform, and selecting switch sections are provided for each individual delay input terminals with output

terminals of the selecting switch sections being connected to the individual delay input terminals and input terminals of the buffer sections being mutually joined.

4. The delay circuit according to claim 1, wherein, in the selecting switch sections, the buffer sections are provided with first transistors whose gate terminals are set as input terminals, and the selecting sections are provided with second transistors into whose gate terminals control signals for establishing the delay path in the delay section are input, and the first and second transistors are connected in series between output terminals of the selecting switch sections and a first power supply voltage.

5. The delay circuit according to claim 4, wherein the first transistors are provided at output terminal side of the selecting switch sections and the second transistors are provided at the first power supply voltage side.

6. The delay circuit according to claim 4, wherein the first transistors are provided at the first power supply voltage side and the second transistors are provided at an output terminal side of the selecting switch sections.

7. The delay circuit according to claim 4, wherein, in the selecting switch sections, the buffer sections are further provided with third transistors whose gate terminals are set as input terminals, and the selecting sections are further provided with fourth transistors into whose gate terminals the control signals for establishing the delay path in the delay section are input, and the third and fourth transistors are connected in series between output terminals of the selecting switch sections and a second power supply voltage.

8. The delay circuit according to claim 7, wherein the first and

third transistors are provided at an output terminal side of the selecting switch sections, the second transistors are provided at the first power supply voltage side, and the fourth transistors are provided at the second power supply side.

9. The delay circuit according to claim 7, wherein the second and fourth transistors are provided at an output terminal side of the selecting switch sections, the first transistors are provided at the first power supply voltage side, and the third transistors are provided at the second power supply side.

10. The delay circuit according to claim 4, wherein the first power supply voltage is a power supply voltage potential and the first and second transistors are PMOS transistors.

11. The delay circuit according to claim 4, wherein the first power supply voltage is a ground potential and the first and second transistors are NMOS transistors.

12. The delay circuit according to claim 7, wherein the second power supply voltage is a power supply voltage potential and the third and fourth transistors are PMOS transistors.

13. The delay circuit according to claim 7, wherein the second power supply voltage is a ground potential and the third and fourth transistors are NMOS transistors.

14. The delay circuit according to claim 4, wherein drive capacity of the second transistors are larger than drive capacity of the first transistors.

15. The delay circuit according to claim 4, wherein drive capacity of the fourth transistors are larger than drive capacity of the third transistors.

16. The delay circuit according to claim 2, wherein, in the delay section, the individual delayed output terminals are connected to input terminals of the next predetermined delay stage and a

plurality of predetermined delay stages are connected in series.

17. The delay circuit according to claim 3, wherein, in the delay section, the output terminals of the predetermined delay stages are connected to the next individual delayed input terminals and a plurality of predetermined delay stages are connected in series.

18. The delay circuit according to claim 16, wherein, in the predetermined delay stages, the rise delay time and fall delay time for an input signal are balanced so as to be substantially uniform.

19. The delay circuit according to claim 18, wherein the predetermined delay stages are formed with a basic unit being a unit delay stage in which an even number of logic inversion sections, in which the rise delay time and fall delay time for an input signal are balanced so as to be substantially uniform, are connected in series.

20. The delay circuit according to claim 19, wherein the logic inversion sections are inverter gates.

21. The delay circuit according to claim 18, wherein the predetermined delay stages are formed with a basic unit being a unit delay stage in which an even number of logic inversion sections, in which the rise delay time and fall delay time of an input signal are different, are connected in series.

22. The delay circuit according to claim 21, wherein the logic inversion sections are NAND gates that form inverted logic through input terminals other than the input terminals into which the propagated signals are input being connected to the power supply voltage potential.

23. The delay circuit according to claim 21, wherein the logic inversion sections are NOR gates that form inverted logic through input terminals other than the input terminals into which the

propagated signals are input being connected to the ground potential.

24. The delay circuit according to claim 16, wherein the delay section is formed from predetermined delay stages each having the same structure.

25. The delay circuit according to claim 4, wherein, when the delay path in the delay section is established using a logic combination of two or more composite control signals, there is provided instead of the second or fourth transistors, transistor series having the same functions as the second or fourth transistors and formed from two or more transistors connected in series into whose respective gate terminals the respective composite control signals are input.

26. A semiconductor integrated circuit device comprising:

a delay section having two or more predetermined delay stages in which a predetermined delay time is added to an input signal;

selecting switch sections;

buffer sections for inputting propagated signals from the input signal; and

selecting sections for establishing a delay path in the delay section;

wherein the selecting switch sections combine the predetermined delay stages as appropriate and establish a delay path for the input signal that outputs a delayed output signal having the desired delay time.

27. The semiconductor integrated circuit device according to claim 26, wherein, in the selecting switch sections, the buffer sections are provided with first transistors whose gate terminals are set as input terminals, and the selecting sections are provided with second transistors into whose gate terminals control

signals for establishing the delay path in the delay section are input, and the first and second transistors are connected in series between output terminals of the selecting switch sections and a first power supply voltage.

28. The semiconductor integrated circuit device according to claim 26, wherein, in the predetermined delay stages, the rise delay time and fall delay time for an input signal are balanced so as to be substantially uniform.

29. A delay method comprising:

a delay step in which predetermined delay times are sequentially added onto an input signal;

an output step in which delay signals are output for each predetermined delay time added in the delay step; and

a selecting step which is only activated when a delay signal having the desired delay time is output in the output step.

30. The delay method according to claim 29, wherein the selecting step includes a step in which the required power is supplied to the output step.

31. The delay method according to claim 29, wherein, in the delay step, the predetermined delay times have a substantially uniform delay time formed by the rise delay time and the fall delay time of the input signal.